TRANSFORMER ISOLATED DRIVER

FIELD OF THE INVENTION

[0001] The present invention relates to a transformer isolated driver, and more particularly to a transformer isolated gate driver with an active switch (For example: a small power MOSFET) so as to achieve reliable transient performance.

BACKGROUND OF THE INVENTION

[0002] The transformer isolated drivers are used for the driving of the high side power switch (For example: a MOSFET). Please refer to Fig. 1, which is the circuit of a transformer isolated driver of the prior art. T1 is an isolation transformer, QM is a switch (a MOSFET), the capacitor C1 is an input capacitor of the transformer T1, and the reference directions of the voltages on the capacitors are shown in Fig. 1, and C3 is an equivalent input capacitor of the switch QM.

[0003] Fig. 2 is the operating waveforms of the circuit shown in Fig. 1. S1 is the waveform of the output signal of the pulse width modulation (PWM) driver, S2 is the waveform of the primary winding of the transformer, and S3 is the output waveform of the transformer. Assuming that in the steady state, the period of the output signal of the PWM driver S1 is T, the duty-cycle is D, the amplitude value is V_I, and the turns ratio of the transformer T1 is 1, then the steady state voltage on the input DC isolation capacitor C1 is DV_I. When S1 is high, S3 is also high, and the amplitude of S3 is (V_I-V_{C1}), that is $(1-D)V_I$. When S1 is low, S2 is negative, and the amplitude of S2 is $(-V_{C1})$, that is $-DV_I$. Thus, the switch QM has a reversed gate driving voltage so as to have a

strong characteristic of anti-interference. However, a shortcoming of the circuit is that when the duty cycle D is larger, the amplitude of S3, which is $(1-D)V_1$, becomes smaller, which might cause the insufficient driving of the switch QM. Therefore, the circuit of this kind of drivers is not suitable for the situations having larger variations of duty cycle.

[0004] Please refer to Fig. 3, which is another transformer isolated driver of the prior art. The polarities of the transformer T1 are shown in Fig. 3, capacitor C1 is an input capacitor at the primary side of the transformer, capacitor C2 is an output capacitor at the secondary side of the transformer, and C3 is the equivalent input capacitor of a power switch QM (a MOSFET). Please refer to Fig.4 for operating waveforms of the circuit shown in Fig. 3, S1 is the waveform of the output signals of the PWM driver, S2 is the waveform on the primary of the transformer, and S3 is the output waveform of the transformer. Assuming that in the steady state, the period of the output signal of the PWM driver S1 is T, the duty-cycle is D, the amplitude value of S1 is V_1, and the turn ratio of the transformer is 1, then the voltage of steady state across the input capacitor C1 at steady state is $V_{C1}=DV_1$, the voltage across the output capacitor C2 is $V_{C2}=DV_1$, and the reference directions of the voltages across these two capacitors are shown in Fig. 3. When S1 is high, S2 and S3 are both high. The amplitude of S2 is $V2=(V_1-V_{C1})$, that is $(1-D)V_1$. The amplitude of S3 is $V_3=(V_2+V_{C2})$, that is V_1. Thus the amplitude of S3 has no relationship with the duty-cycle D, and keeps unchanged as V_1 at any duty-cycle operating condition. When S1 becomes zero, the input/output voltages of the transformer becomes $-DV_1$,

thus the diode DR is conducted, and the voltage across the equivalent input capacitor C3 of the switch QM is kept zero.

[0005] However, the still existed drawback of the above-mentioned transformer isolated drivers is: that when the driving signal S1 is disappeared due to certain reasons, S3 will become zero immediately as mentioned above. But latter on, the input of the transformer T1 is crossed by the bias of voltage ($-DV_1$) from the capacitor C1, and will be saturated gradually, thus the amplitude of the input/output voltages of the transformer T1 will become smaller starting from DV_1. Since the voltage across the capacitor C2, is still DV_1, therefore, the voltage across the equivalent input capacitor C3 of the switch QM will be increased starting from zero. Until the transformer T1 is saturated, then the primary and secondary side voltages of the transformer T1 will become zero, and the voltage across C3 will finally become DV_1, which will cause the switch QM to suffer a mis-triggering in a longer time resulting in circuit damage. Please refer to Fig.5 for the recorded operating waveform of S3 under circuit protection operating. Therefore, this kind of driving circuits does not have a better transient operating. When a power converter implemented with this driver is started up or is shut down, the power switch will suffer a mis-triggering, thus causing the break down of the whole power converter.

SUMMARY OF THE INVENTION

[0006] It is therefore an object of the present invention to provide a transformer isolated gate driver with an active switch (a small power MOSFET) for driving of a power switch with reliable transient performance, and avoiding the power switch from suffering

mis-triggering so as to prevent the break down of the whole power converter.

[0007] According to the aspect of the present invention, the transformer isolated gate driver electrically connected to a power switch for realizing the driving of the power switch includes: a PWM driver for producing a PWM signal; a transformer electrically connected to the PWM driver; an input capacitor electrically connected to a primary side of the transformer in series; an output capacitor electrically connected to a secondary side of the transformer in series; an output diode electrically connected to two output terminals of the transformer isolated gate driver in parallel; an active switch electrically connected to the output capacitor in series and having an input electrode electrically connected to a first terminal of the secondary side of the transformer, and a first electrode electrically connected to a second terminal of the secondary side of the transformer; and the secondary side of the transformer, the output capacitor, the output diode, and the active switch are electrically connected in series, and when the PWM signal is disappeared, by discharging a plurality of charges across an equivalent input capacitor of the power switch through the secondary side of the transformer, the output capacitor, and a body diode of the active switch, a driving signal on the power switch is disappeared.

[0008] Preferably, the two polarities of the transformer are the same.

[0009] Preferably, the two polarities of the primary and secondary windings of the transformer are reversed.

[0010] Preferably, the power switch is a MOSFET.

[0011] Preferably, the active switch is a small power MOSFET, and the input electrode, the first electrode, and the second electrode of the active switch are a gate, a source, and a drain of a MOSFET respectively.

[0012] Preferably, the output capacitor is electrically connected between a cathode of the output diode and the input electrode of the active switch.

[0013] Preferably, the output capacitor is electrically connected between an anode of the output diode and the second electrode of the active switch.

[0014] Preferably, one selected from a group consisting of the input capacitor, the output capacitor, and the two output terminals of the transformer isolated gate driver is electrically connected to a resistor in parallel selectively.

[0015] Preferably, an input diode is electrically connected to the input capacitor in parallel, wherein an anode of the input diode is connected to a first end of the input capacitor connecting with the primary winding of the transformer, and a cathode of the input diode is connected to a second end of the input capacitor.

[0016] According to another aspect of the present invention, a transformer isolated circuit electrically connected to a PWM driver and a power switch for realizing the driving of the power switch includes: a transformer; an input capacitor electrically connected to a primary winding of the transformer in series; an output capacitor electrically connected to a secondary side of the transformer in series; an output diode electrically connected to two output terminals of the transformer

isolated gate driver in parallel; an active switch electrically connected to the output capacitor in series and having an input electrode electrically connected to a first terminal of the secondary side of the transformer, and a first electrode electrically connected to a second terminal of the secondary side of the transformer; and the secondary side of the transformer, the output capacitor, the output diode, and the active switch are electrically connected in series.

[0017] Preferably, the two polarities of the primary and secondary windings of the transformer are the same.

[0018] Preferably, the two polarities of the primary and secondary windings of the transformer are reversed.

[0019] The present invention may best be understood through the following descriptions with reference to the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Fig. 1 is the circuit diagram of the transformer isolated driver of the prior art;

[0021] Fig. 2 is the operation waveforms of the transformer isolated driver shown in Fig. 1;

[0022] Fig. 3 is the circuit diagram of another transformer isolated driver of the prior art;

[0023] Fig. 4 is the operation waveforms of the transformer isolated driver shown in Fig. 3;

[0024] Fig. 5 is the experimental waveform of the output driving signal when the PWM signal is disappeared regarding the circuit shown in Fig. 3;

[0025] Fig. 6 is the circuit diagram of the first preferred embodiment of the transformer isolated driver of the present invention;

[0026] Fig. 7 is the experimental waveform of the output driving signal when the PWM signal is disappeared regarding the circuit shown in Fig. 6;

[0027] Fig. 8 is the circuit diagram of the second preferred embodiment of the transformer isolated driver of the present invention; and

[0028] Fig. 9 is the circuit diagram of the third preferred embodiment of the transformer isolated driver of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0029] Please refer to Fig. 6, which is the first preferred embodiment of the transformer isolated gate driver of the present invention. The transformer isolated driver for realizing the driving of a power switch QM (a MOSFET) includes a PWM driver for producing PWM signal, a transformer T1 having polarities of primary winding and secondary winding as shown in the figure, an input capacitor C1 and an output capacitor C2 connected to the primary/secondary windings of the transformer T1 in series respectively for blocking DC components, an active switch Q1 (a small power MOSFET), and an output diode D1 connected to the two output terminals of the transformer isolated driver in parallel. Meanwhile, the active switch Q1 is connected to the output capacitor C2 in series, the input electrode (gate) of the active switch Q1 is connected to the first terminal of the secondary winding of the transformer T1, the first electrode (source) of the active switch Q1 is connected to the second terminal of the secondary winding of the

transformer T1. A series connected circuit is constructed by the output capacitor C2, the output diode D1, and the active switch Q1. And the input electrode (gate) of the power switch QM (a MOSFET) is connected to the cathode of the output diode D1. The first electrode (source) of the power switch QM is connected to the anode of the output diode D1.

[0030] When this driving circuit of Fig. 6 is operating in steady state, the operation waveforms are the same as the waveforms shown in Fig. 2. If the amplitude of the driving signal switch comes from the PWM driver, is V_1, and the duty-cycle of the driving signal is D, then the voltage across the input capacitor C1, is $V_{C1}=DV_1$. Assuming that the turnratio of the transformer T1 is 1, then the voltage across the output capacitor C2 is $V_{C2}=DV_1$. When the driving signal S1 is high, the output voltage of the secondary winding of the transformer T1 is also high and the amplitude is $(1-D)V_1$. During above period, the active switch Q1 is kept in conducting, and the amplitude of the output voltage S3 to the power switch QM is $(V_{C2}+(1-D)V_1)$, that is V_1. When the driving signal S1 becomes zero, the voltage across the primary winding of the transformer S2 is $(-DV_1)$, the gate voltage of the active switch Q1 is also $(-DV_1)$, and the active switch Q1 is switched off. At the mean time, the parasitical body diode of the active switch Q1 is forwardly conducted, and the output diode D1 is conducted also, thus the charges on C3 can be discharged through this short-circuit quickly, and the amplitude of the output waveform of the transformer isolated driver S3 will become zero immediately.

[0031] When the power converter is shutdown from off operation or from circuit failure protection, the driving signal S1 will be pulled to zero.

During the period of shutdown, the voltage across the primary winding of the transformer T1 will become $-V_{C1}$, the active switch Q1 is switched off, and the voltage across the output capacitor C2 will be kept as $V_{c2}=DV_1$ at the moment. Thus, the sum of voltage across the secondary winding of transformer T1 and that across the output capacitor C2 will become zero, the charges on the equivalent input capacitor C3 of the power switch will be discharged through the output capacitor C2, the output terminal of the transformer and the body diode of the active switch Q1, and the voltage across C3 will become zero quickly. After that, voltage from the input capacitor C1 crossed by the primary winding of the transformer T1 is continuously, the transformer T1 will go into saturation, and the voltages across the primary and the secondary winding of the transformer will decrease to zero gradually as same as that of the circuit shown in Fig. 3. During this stage, the input electrode (gate) and the first electrode (source) of the active switch Q1 accept a zero voltages, thus the active switch Q1 is sustained at a switched off status , and the voltage across input capacitor C3 of the power switch QM will be kept zero, thus there will be no more mis-triggering problem like that in the circuit shown in Fig. 3.

[0032] Therefore, the adding of the active switch Q1 maintains normal operation of the transformer isolated driver under steady states, and meanwhile effectively prevent the mis-triggering to the power switch as that of the prior art, and achieves reliable transient operation when PWM signal is pulled to zero due to off operation or failure protection of the power converter. Please refer to Fig. 7, which is the experimental result of the output waveforms of the transformer isolated gate driver of

the present invention when the PWM signal is pulled to zero from normal operation.

[0033] It is understandable, though the above-mentioned is a preferred embodiment of the present invention, there could be other preferred embodiments. For examples, the transformer isolated drivers could also be implemented as that shown in Fig. 8 or in Fig. 9. Please refer to Fig. 8, the difference between this preferred embodiment and the first preferred embodiment of Fig. 6 is that nominal terminals of the transformer shown in Fig. 8 are in reverse but the polarities of the transformer shown in Fig. 6 are the same. Thus the output driving signal of the transformer isolated driver in Fig. 8 and the output driving signal of the transformer isolated driver in Fig. 6 are in reverse phase. Please refer to Fig. 9 for another preferred embodiment, the nominal terminals of the transformer can be either that of Fig. 6 or that of Fig. 8, and the main difference is that the output capacitor C2 is connected in series between the anode of diode D1 and the second electrode (drain) of the active switch Q1. Among the preferred embodiments of Fig. 8 and Fig. 9, a series connected circuit is formed by the secondary winding of the transformer, the output capacitor, the output diode and the active switch in both cases. Besides, additional resistors can be further connected to the input capacitor C1, the output capacitor C2, and the output terminals in parallel. Among the preferred embodiments of Fig. 6, Fig. 8, and Fig. 9, a diode can be connected to the input capacitor C1 in parallel, the anode of the diode is connected to the connecting terminal of the input capacitor C1 and the transformer T1, and the cathode of the diode is connected to the other terminal of the input capacitor C1 thus

suppressing the ring voltage across the windings of T1 and avoiding the miss triggering of Q1.

[0034] While the invention has been described in terms of what are presently considered to be the most practical and preferred embodiments, it is to be understood that the invention need not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims that are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structure.